In The Claims:

Please amend the claims as follows:

1. (Original) A method for forming a wire line by a damascene process, the method comprising:

forming a first insulating layer on a semiconductor substrate;

etching the first insulating layer to form a contact hole;

forming a first conductive layer over the first insulating layer that fills the contact hole;

patterning the first conductive layer;

forming a storage node contact that fills the contact hole and is electrically connected to the semiconductor substrate;

forming a hard mask over the storage node contact;

etching the first insulating layer using the hard mask as an etch mask to form a trench in the first insulating layer;

forming a bit line that is electrically connected to the semiconductor substrate in the trench;

forming a second insulating layer that covers the bit line;

planarizing the second insulating layer and the hard mask; and

forming a storage node on the storage node contact.

2. (Original) The method of claim 1, further comprising forming a transistor on the semiconductor substrate, wherein the bit line and the storage node contact are electrically connected to the transistor.

3. (Original) The method of claim 1, wherein the first conductive layer is formed of a conductive material by which an etch selectivity to the first insulating layer can be obtained.

4. (Original) The method of claim 3, wherein in order to obtain the etch selectivity, the first conductive layer is formed of polysilicon, and the first insulating layer is formed of silicon oxide.

5. (Original) The method of claim 1, wherein the hard mask extends in a line shape and is connected to the storage node contact.

6. (Original) The method of claim 1, wherein the hard mask is formed to a critical dimension (CD) narrower than a top CD of the contact hole.

7. (Original) The method of claim 1, wherein the step of patterning the first conductive layer comprises:

forming a photoresist pattern over the first conductive layer, the photoresist pattern having a line shape that overlaps the contact hole; and

etching the first conductive layer using the photoresist pattern as an etch mask so that a top surface of the first insulating layer is exposed.

8. (Original) The method of claim 1, further comprising forming a trench spacer on a sidewall of the trench.

9. (Original) The method of claim 8, wherein the trench spacer is formed of silicon oxide.

10. (Original) The method of claim 1, wherein the step of forming a bit line comprises:

forming a second conductive layer of a material different from that of the first conductive layer over the trench; and

etching the second conductive layer selectively so that a surface of the second conductive layer is lower than an entrance of the trench.

11. (Original) A method for forming a wire line by a damascene process, the method comprising:

forming a first insulating layer on a semiconductor substrate;

etching the first insulating layer to form a contact hole;

forming a first conductive layer that fills the contact hole over the first insulating layer;

patterning the first conductive layer;

forming a storage node contact that fills the contact hole and is electrically connected to the semiconductor substrate;

forming a hard mask over the storage node contact;

taper-etching the first insulating layer using the hard mask as an etch mask to form a trench, the trench having a tilted sidewall and being separated from the contact hole by a barrier wall formed of a remaining portion of the first insulating layer;

forming a bit line that is electrically connected to the semiconductor substrate, in the trench;

forming a second insulating layer that covers the bit line;

planarizing the second insulating layer and the hard mask; and

forming a storage node on the storage node contact.

12. (Original) The method of claim 11, further comprising forming a transistor on the semiconductor substrate, wherein the bit line and the storage node contact are electrically connected to the transistor.

13. (Original) The method of claim 11, wherein the contact hole is formed by a taper etch process so as to extend a width of the barrier wall.

14. (Original) The method of claim 11, wherein the first conductive layer is formed of a conductive material by which an etch selectivity to the first insulating layer can be obtained.

15. (Original) The method of claim 11, further comprising forming a trench spacer on the barrier wall.

16. (Original) The method of claim 11, wherein the step of forming a bit line comprises:

forming a second conductive layer of a material different from that of the first conductive layer over the trench; and

etching the second conductive layer selectively so that a surface of the second conductive layer is lower than an entrance of the trench.

17. (Original) A method for forming a wire line by a damascene process, the method comprising:

forming a first insulating layer on a semiconductor substrate;

taper-etching the first insulating layer to form a contact hole having a tilted sidewall;

forming a first conductive layer over the first insulating layer that fills the contact hole;

patterning the first conductive layer;

forming a storage node contact that fills the contact hole and is electrically connected to the semiconductor substrate;

forming a hard mask over the storage node contact;

taper-etching the first insulating layer using the hard mask as an etch mask to form a trench, the trench having a tilted sidewall and being separated from the contact hole by a barrier wall formed of a remaining portion of the first insulating layer;

forming a bit line that is electrically connected to the semiconductor substrate in the trench;

forming a second insulating layer that covers the bit line;

planarizing the second insulating layer and the hard mask; and

forming a storage node on the storage node contact.

18. (Currently Amended) A method for forming a wire line by a damascene process, the method comprising:

forming a first insulating layer on a semiconductor substrate;

etching the first insulating layer to form a contact hole having a tilted sidewall;

forming a polysilicon layer over the first insulating layer that fills the contact hole;

patterning the polysilicon layer;

forming a storage node contact that fills the contact hole and is electrically connected to the semiconductor substrate;

forming a hard mask over the storage node contact;

etching the first insulating layer using the hard mask as an etch mask to form a trench in the first insulating layer;

forming an etch stopper of titanium nitride over sidewalls of the trench;

forming a tungsten layer that over the etch stopper that fills the trench;

etching the tungsten layer selectively so that a portion of the etch stopper formed over sidewalls of the trench is exposed and the tungsten layer is recessed in the trench to form a bit line that is electrically connected to the semiconductor substrate;

removing the exposed portion of the etch stopper;

forming a second insulating layer that covers the bit line;

planarizing the second insulating layer and the hard mask; and

forming a storage node on the storage node contact.

19. (Original) The method of claim 18, wherein the etch stopper extends to cover the hard mask.

20. (Original) A method for forming a wire line by a damascene process, the method comprising:

forming a first insulating layer on a semiconductor substrate;

taper-etching the first insulating layer to form a contact hole having a tilted sidewall;

forming a polysilicon layer over the first insulating layer that fills the contact hole;

patterning the polysilicon layer;

forming a storage node contact that fills the contact hole and is electrically connected to the semiconductor substrate;

forming a hard mask over the storage node contact;

taper-etching the first insulating layer using the hard mask as an etch mask to form a trench, the trench having tilted sidewalls and being separated from the contact hole by a barrier wall formed of a remaining portion of the first insulating layer;

forming an etch stopper of titanium nitride over sidewalls of the trench;

forming a tungsten layer that fills the trench;

etching the tungsten layer selectively so that a portion of the etch stopper formed over sidewalls of the trench is exposed and the tungsten layer is recessed in the trench to form a bit line that is electrically connected to the semiconductor substrate;

removing the exposed portion of the etch stopper;

forming a second insulating layer that covers the bit line;

planarizing the second insulating layer and the hard mask; and

forming a storage node on the storage node contact.

21. (Canceled)

22. (Currently Amended) ~~The method of claim 21,~~ A method for forming a wire line by a damascene process, the method comprising:

forming an insulating layer over a semiconductor substrate;

forming a contact hole in the first insulating layer;

forming a storage node contact that fills the contact hole and is electrically connected to the semiconductor substrate;

forming a hard mask over the storage node contact;

etching the insulating layer using the hard mask as an etch mask to form a trench in the insulating layer; and

forming a bit line that is electrically connected to the semiconductor substrate in the trench,

wherein the storage node contact and the hard mask are formed simultaneously.

23. (Original) The method of claim 22, wherein the step of forming the storage node contact and the hard mask comprises:

forming a first conductive layer over the insulating layer, the first conductive layer filling the contact hole;

forming a photoresist pattern over the first conductive layer, the photoresist pattern overlapping the contact hole; and

etching the conductive layer using the photoresist pattern as an etch mask so that a top surface of the first insulating layer is exposed.

24. (Currently Amended) The method of claim 23, wherein the step of forming a bit line comprises:

forming a second conductive layer of a material different from that of the first conducting layer over the trench; and

etching the second conductive layer selectively so that a surface of the second conductive layer is lower than an entrance of the trench.